

1 WHAT IS CLAIMED IS:

2 1. A semiconductor packaging structure comprising:

3 a metal lead frame having a die pad and having a plurality of leads
4 arranged around the die pad, wherein the metal lead frame has multiple gaps
5 and each gap is defined by an adjacent two of the plurality of leads, and the
6 multiple gaps are filled with an isolating resin;

7 a wall portion formed on the metal lead frame and positioned along a
8 periphery of the metal lead frame;

9 a chip mounted on the die pad of the metal lead frame and electrically
10 connected to the plurality of leads; and

11 a cover mounted on the wall portion to enclose the chip inside the wall
12 portion.

13 2. The semiconductor packaging structure as claimed in claim 1 further
14 having multiple notches and each notch is defined on a bottom surface of the
15 metal lead frame and is communicated with one of the multiple gaps, wherein
16 each notch and gap are filled with the isolating resin.

17 3. The semiconductor packaging structure as claimed in claim 1, wherein
18 the die pad is higher than of the plurality of leads, whereby a space is defined
19 below the die pad to receiving the isolating pad.

20 4. The semiconductor packaging structure as claimed in claim 2, wherein
21 the cover is a transparent cover.

22 5. The semiconductor packaging structure as claimed in claim 3, wherein
23 the cover is a transparent cover.

24 6. The semiconductor packaging structure as claimed in claim 2, wherein

1 the cover is a metal cover.

2 7. The semiconductor packaging structure as claimed in claim 3, wherein
3 the cover is a metal cover.

4 8. The semiconductor packaging structure as claimed in claim 4, wherein
5 the wall portion is formed of the isolating resin, and the wall portion is
6 integrally formed with the isolating resin that fills the multiple gaps.

7 9. The semiconductor packaging structure as claimed in claim 5, wherein
8 the wall portion is formed of the isolating resin, and the wall portion is
9 integrally formed with the isolating resin that fills the multiple gaps.

10 10. A semiconductor packaging structure comprising:

11 a metal lead frame composed of an upper lead frame and a lower lead
12 frame, wherein

13 the upper lead frame has a first die pad, a first plurality of leads
14 arranged around the first die pad, a first interval defined between the first
15 die pad and the first plurality of leads, and a first plurality of gaps each is
16 defined by an adjacent two of the first plurality of leads and is
17 communicated with the first interval;

18 the lower lead frame has a second die pad, a second plurality of leads
19 arranged around the second die pad, a second interval defined between
20 the second die pad and the second plurality of leads, and a second
21 plurality of gaps, each of the second plurality of gaps is defined by two
22 adjacent of the second plurality of leads and is communicated with the
23 second interval, wherein when the upper lead frame and the upper lead
24 frame are compressed together, the first interval, the second interval, the

1 first and the second plurality of gaps are communicated with each other
2 for receiving an isolating resin;
3 a wall portion formed around a periphery of the upper lead frame;
4 a chip mounted on the first die pad of the upper lead frame and
5 electrically connected to the first plurality of leads; and
6 a cover mounted on the wall portion to enclose the chip inside the wall
7 portion.

8 11. The semiconductor packaging structure as claimed in claim 10,
9 wherein the second die pad is slightly smaller than the first die pad.

10 12. The semiconductor packaging structure as claimed in claim 10,
11 wherein each of the first plurality of leads has an external portion extending
12 toward a flange of the upper lead frame, and has an internal portion extending
13 toward the first die pad, each of the second plurality of leads corresponds to
14 the external portion of one of the first plurality of leads.

15 13. The semiconductor packaging structure as claimed in claim 11,
16 wherein each of the first plurality of leads has an external portion extending
17 toward a flange of the upper lead frame, and has an internal portion extending
18 toward the first die pad, each of the second plurality of leads corresponds to
19 the external portion of one of the first plurality of leads.

20 14. The semiconductor packaging structure as claimed in claim 10,
21 wherein the upper lead frame and the lower lead frame each further has a
22 metal film electroplated thereon.

23 15. The semiconductor packaging structure as claimed in claim 10,
24 wherein the cover is a transparent cover.

1 16. The semiconductor packaging structure as claimed in claim 10,
2 wherein the cover is a metal cover.

3 17. The semiconductor packaging structure as claimed in claim 13,
4 wherein the cover is a transparent cover.

5 18. The semiconductor packaging structure as claimed in claim 13,
6 wherein the cover is a metal cover.

7 19. A semiconductor packaging structure comprising:
8 a metal lead frame having a die pad and having a plurality of leads
9 arranged around the die pad, wherein the metal lead frame has multiple gaps
10 and each gap is defined by an adjacent two of the plurality of leads, and the
11 multiple gaps are filled with an isolating resin;

12 a wall portion formed on the metal lead frame and positioned along a
13 periphery of the metal lead frame;

14 a chip mounted on the die pad of the metal lead frame and electrically
15 connected to the plurality of leads; and

16 a transparent resin putted inside the wall portion to enclose the chip
17 inside the wall portion.

18 20. The semiconductor packaging structure as claimed in claim 19
19 further having multiple notches and each notch is defined on a bottom surface
20 of the metal lead frame and is communicated with one of the multiple gaps,
21 wherein each notch and gap are filled with the isolating resin.